P21699.A25

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant	: Kazuyuki OHHASHI	Confirmation No.: 8111
Appln. No.	: 09/988,208	Examiner: F.N. Aghdam
Filed	: November 19, 2001	Group Art Unit: 2611
For	: PHASE OFFSET CALCULATION METHOD AND PHASE OFFSET CIRCUIT	

APPEAL BRIEF UNDER 37 C.F.R. §41.37

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Appeal Brief - Patents
Randolph Building
401 Dulany Street
Alexandria VA 22314

Sir:

This appeal is from the rejection of claims 25-31 and 33-35 under 35 U.S.C. §103(a), as set forth in the Final Office Action of April 29, 2009, and as maintained in the Advisory Action dated August 5, 2009.

A Notice of Appeal, a Request for (one-month) Extension of Time, and a Pre-Appeal Brief Request for Review were filed on August 31, 2009 in response to the Final Office Action of April 29, 2009, and the one-month period for filing an Appeal Brief following a Panel Decision from Pre-Appeal Brief Review dated October 6, 2009 was set to expire on November 6, 2009.

The requisite fee for filing an Appeal Brief under 37 C.F.R. §41.20(b) (2) is submitted concurrently herewith. However, if for any reason the necessary fee is not associated with this file or the concurrently submitted fee is inadequate, the Commissioner is authorized to charge the

fee for the Appeal Brief and any necessary extension of time fees to Deposit Account No. 19-0089.

(1) **REAL PARTY IN INTEREST**

The real party in interest is Panasonic Corporation, as evidenced by a Change of Name recorded in the U.S. Patent and Trademark Office on November 21, 2008, at Reel 021897 and Frame 0624.

(2) **RELATED APPEALS AND INTERFERENCES**

No related appeals and/or interferences are pending.

(3) **STATUS OF THE CLAIMS**

Claims 25-31 and 33-35, all of the claims pending in this application, stand finally rejected and are the subject of this appeal. Appellant appeals the final rejection of claims 25-31 and 33-35. A copy of claims 25-31 and 33-35 is attached as an Appendix to this brief.

Claims 1-24 and 32 are cancelled.

(4) **STATUS OF THE AMENDMENTS**

Claim 32 was cancelled in a Response Under 37 C.F.R. § 1.116 filed on July 20, 2009 after the final rejection of April 29, 2009.

(5) **SUMMARY OF THE CLAIMED SUBJECT MATTER**

Initially, Appellant notes that the following descriptions are made with respect to the independent claims and include references to particular parts of the specification. As such, the

following are merely exemplary and are not a surrender of other aspects of the present invention that are also enabled by the present specification as well as those that are directed to equivalent structures or methods.

Independent claim 25 recites a phase offset calculator, comprising: a sign inverter that inverts a sign of signed binary data to obtain a first phase offset of a multiple of 90°; an amplitude adjuster that adjusts an amplitude of a signal output from the sign inverter; and a phase offsetter that provides a second phase offset smaller than 90° to a signal output from the amplitude adjuster.

In this regard, exemplary embodiments of the present specification are shown in Figures 4A and 5-8 and disclosed at pages 9-19, and particularly in embodiments disclosed with respect to Figures 4A and 5-8 at page 9, line 25 to page 11, line 1 and page 11, line 27 to page 19, line 13. The exemplary embodiments disclose a phase offset calculator (Figure 4A), comprising: a sign inverter (#401) that inverts a sign of signed binary data to obtain a first phase offset of a multiple of 90°; an amplitude adjuster (#402) that adjusts an amplitude of a signal output from the sign inverter (#401); and a phase offsetter (#403) that provides a second phase offset smaller than 90° to a signal output from the amplitude adjuster (#402).

Independent claim 26 recites a signal point mapper for mapping a QPSK modulation signal in a phase space, comprising: a sign inverter that inverts a sign of the QPSK modulation signal to obtain a first phase offset of a multiple of 90°; an amplitude adjuster that adjusts an amplitude of a signal output from the sign inverter; and a phase offsetter that provides a second phase offset smaller than 90° to a signal output from the amplitude adjuster.

In this regard, exemplary embodiments of the present specification are shown in Figures 4A and 5-8 and disclosed at pages 9-19, and particularly in embodiments disclosed with respect

to Figures 4A and 5-8 at page 9, line 25 to page 11, line 1 and page 11, line 27 to page 19, line 13. The exemplary embodiments disclose a signal point mapper (Figures 5 and 7, #40) for mapping a QPSK modulation signal in a phase space, comprising: a sign inverter (#60) that inverts a sign of the QPSK modulation signal to obtain a first phase offset of a multiple of 90°; an amplitude adjuster (#61) that adjusts an amplitude of a signal output from the sign inverter (#60); and a phase offsetter (#62) that provides a second phase offset smaller than 90° to a signal output from the amplitude adjuster (#61).

Independent claim 28 recites a CDMA transmission apparatus for controlling a phase and amplitude of a transmission signal by closed-loop control, comprising: a signal point mapper having: a sign inverter that inverts a sign of a QPSK modulation signal to obtain a first phase offset of a multiple of 90°; an amplitude adjuster that adjusts an amplitude of a signal output from the sign inverter; and a phase offsetter that calculates a second phase offset smaller than 90° with a signal output from the amplitude adjuster; and a transmission controller that provides control information to the signal point mapper based on a message included in a reception signal from a receiver that receives communication signals from the CDMA transmission apparatus.

In this regard, exemplary embodiments of the present specification are shown in Figures 4A and 5-8 and disclosed at pages 9-19, and particularly in embodiments disclosed with respect to Figures 4A and 5-8 at page 9, line 25 to page 11, line 1 and page 11, line 27 to page 19, line 13. The exemplary embodiments disclose a CDMA transmission apparatus (Figure 5, #10) for controlling a phase and amplitude of a transmission signal by closed-loop control, comprising: a signal point mapper (Figures 5 and 7, #40) having: a sign inverter (#60) that inverts a sign of a QPSK modulation signal to obtain a first phase offset of a multiple of 90°; an amplitude adjuster (#61) that adjusts an amplitude of a signal output from the sign inverter (#60); and a phase

offsetter (#62) that calculates a second phase offset smaller than 90° with a signal output from the amplitude adjuster (#61); and a transmission controller (Figure 5, #18) that provides control information to the signal point mapper (Figures 5 and 7, #40) based on a message included in a reception signal from a receiver (Figure 5, R1 to Rn) that receives communication signals from the CDMA transmission apparatus (#10).

Independent claim 33 recites a phase offsetter, comprising: a sign inverter that inverts a sign of signed binary data to obtain a first phase offset of a multiple of 90°; and a phase shifter that calculates a phase shift to provide the sign-inverted signed binary data a phase offset smaller than 90°, and that provides the sign-inverted signed binary data the phase offset smaller than 90° based on a control signal from a remote source.

In this regard, exemplary embodiments of the present specification are shown in Figures 1, 2A and 2B and disclosed at pages 6-9, and particularly in embodiments disclosed with respect to Figures 1, 2A and 2B at page 6, line 24 to page 9, line 24. The exemplary embodiments disclose a phase offsetter (#200), comprising: a sign inverter (#210) that inverts a sign of signed binary data to obtain a first phase offset of a multiple of 90°; and a phase shifter (#220) that calculates a phase shift to provide the sign-inverted signed binary data a phase offset smaller than 90°, and that provides the sign-inverted signed binary data the phase offset smaller than 90° based on a control signal from a remote source (Figure 2A, "Control Signal", page 9, lines 19-21).

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Decision to Reject Claims 25-31 and 33-35 under 35 U.S.C. §103(a), over SATO (U.S. Patent No. 5,956,328), in view of Appellant's disclosed prior art.

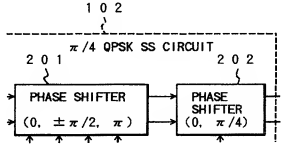
(7) **ARGUMENT**

The Decision to Reject Claims 25-31 and 33-35 under 35 U.S.C. §103(a), over SATO (U.S. Patent No. 5,956,328), in view of Appellant's disclosed prior art, is Improper, and the Decision to Reject Claims 25-31 and 33-35 on this Ground Should be Reversed.

SATO and Appellant's disclosed prior art

In the Final Office Action, claims 25-31 and 33-35 were rejected under 35 U.S.C. §103(a), over SATO (U.S. Patent No. 5,956,328), in view of Appellant's disclosed prior art. A summary explanation of the teachings of SATO and Appellant's disclosed prior art is provided below prior to a discussion of the differences between the features recited in the pending claims and SATO, and Appellant's disclosed prior art.

SATO discloses, at Figures 1 and 2, a QPSK spreading circuit 102 that includes phase shifters 201 and 202. The QPSK spreading circuit of SATO appears as follows in Figure 1:



Appellant's disclosed prior art is shown in Figure 4B of Appellant's specification, and includes an amplitude multiplier 406 and phase offset calculator 407. The amplitude multiplier and phase offset calculator of Appellant's disclosed prior art are shown as follows in Figure 4B:

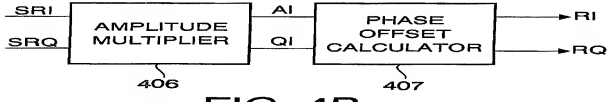


FIG. 4B
(PRIOR ART)

Claim 25

Claim 25 is directed to a phase offset calculator that includes the following components: comprising:

- a sign inverter that inverts a sign of signed binary data to obtain a first phase offset of a multiple of 90°;
- an amplitude adjuster that adjusts an amplitude of a signal output from the sign inverter; and
- a phase offsetter that provides a second phase offset smaller than 90° to a signal output from the amplitude adjuster.

That is, an amplitude adjuster in claim 25 adjusts an amplitude of a signal output from a sign inverter, and feeds a signal to the phase offsetter. These features are readily shown in Figure 4A.

As explained in Appellant's specification at page 11, the content of phase offset processing using only phase offset calculator 407 in Appellant's disclosed prior art shown in Figure 4B is as follows:

$RI = AI\cos\theta + AQ\sin\theta$, $RQ = AI\cos\theta - AQ\sin\theta$ ... (2).

Appellant further describes, at page 11, that the configuration of Appellant's embodiment shown in Figure 4A can be used to simplify the above-noted signal processing of the disclosed prior art phase offset calculator 407 shown in Figure 4B. The arrangement of elements recited in Appellant's claims is not simply a rearrangement of parts. Rather, the arrangement of elements in Appellant's claims effects complex signals and signal processing, and the signals and signal

processing resulting from the arrangement of elements in Appellant's embodiments are discussed at length in Appellant's specification.

The rejection of claim 25 is based on the premise that it would be obvious to one or ordinary skill in the art to modify a QPSK spreading circuit 102 in SATO with teachings of Appellant's disclosed prior art shown in Figure 4B to result in Appellant's claimed invention. This rejection is incorrect, and reflects a misunderstanding of Appellant's claimed invention as a simple arrangement and re-arrangement of known mechanical parts without regard to the signals and signal processing that relate to the claimed elements and their arrangement.

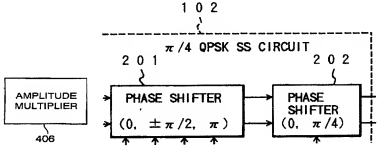
The combination of SATO and Appellant's disclosed prior art would not result in the combination of claim 25. Additionally, claim 25 is not rendered obvious by SATO in view of Appellant's disclosed prior art. Finally, the Examiner has reconstructed Appellant's claimed invention together impermissibly in hindsight, using Appellant's disclosure as a roadmap to combine SATO and Appellant's disclosed prior art in a way unrelated entirely to the teachings of either SATO or Appellant's disclosed prior art.

The Examiner has not and cannot provide any proper interpretation of how SATO and Appellant's disclosed prior art would or could be combined such that Appellant's claims would result. Indeed, during prosecution of this application, Appellant has provided numerous potential interpretations of the proposed combination of SATO and Appellant's disclosed prior art, but the interpretations provided by Appellant are the only interpretations of potential combinations provided during the prosecution of this application. Therefore, the Examiner has not established a prima facie obviousness rejection of Appellant's claim 25, as there is no proper explanation in the record as to how SATO could be modified with Appellant's disclosed prior art so as to obtain the combination of claim 25.

That is, a QPSK spreading circuit 102 in SATO is analogous to phase offset calculator 407 in Appellant's disclosed prior art. The entirety of the functionality of QPSK spreading circuit 102 in SATO is analogous to the entirety of the functionality of phase offset calculator 407 in Appellant's disclosed prior art, in that both elements are the phase offset/shifting units in their respective arrangements shown. Neither SATO nor Appellant's disclosed prior art discloses an amplitude adjuster that both adjusts an amplitude of a signal output from a sign inverter, and feeds a signal to a phase offsetter. Put another way, neither SATO nor Appellant's disclosed prior art includes an amplitude adjuster that provides processing intermediate processing of a sign inverter and a phase offsetter.

Further, using phase offset calculator 407 in Appellant's disclosed prior art to replace the only analogous element of SATO, i.e., by replacing QPSK spreading circuit 102 in SATO with the phase offset calculator 407 in Appellant's disclosed prior art, would not result in the combination of Appellant's claim 25. During prosecution, Appellant provided the following explanations on possible combinations of SATO and Appellant's disclosed prior art, and explained how each such combination does not result in the combination of Appellant's claims.

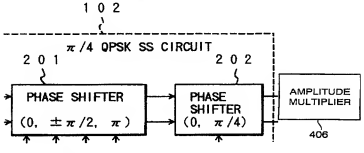
A modification of SATO with teachings of Appellant's disclosed prior art could result in a configuration in which amplitude multiplier 406 is provided to SATO, so that amplitude multiplier 406 performs signal processing prior to QPSK spreading circuit 102, as follows:



That is, the amplitude multiplier 406 in Appellant's disclosed prior art could be placed in front of QPSK spreading circuit 102 in SATO, and then signal amplifier 106 in SATO could be eliminated. There is no conceivable reason in the record for one of ordinary skill in the art to modify SATO in this manner. Further, such a modification does not result in the combination recited in claim 25.

Explained in the alternative, the above configuration might be considered as using QPSK spreading circuit 102 in SATO to replace the phase offset calculator 407 in Appellant's disclosed prior art. However, there is no conceivable reason in the record for one of ordinary skill in the art to modify SATO in this manner. Further, such a modification does not result in the combination recited in claim 25.

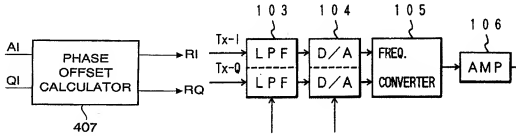
As an alternative, SATO could also be modified in the following manner:



Here, phase offset calculator 407 in Appellant's disclosed prior art could be replaced with QPSK spreading circuit 102 from SATO, and QPSK spreading circuit 102 in SATO would then be placed in front of amplitude multiplier 406 in Appellant's disclosed prior art rather than behind amplitude multiplier 406. However, there is no conceivable reason in the record for one of ordinary skill in the art to modify SATO in this manner. Further, such a modification does not result in the combination recited in claim 25.

That is, with respect to the configuration immediately above, Figure 1 of SATO already shows power amplifier 106 after the QPSK spreading circuit 102, so there is no reason to replace power amplifier 106 in SATO with amplitude multiplier 406 in Appellant's disclosed prior art. Nevertheless, any such combination of SATO and Appellant's disclosed prior art also would not result in Appellant's claimed invention.

Another possible combination of SATO and Appellant's disclosed prior art would result in a configuration such as the following:



Here, phase offset calculator 407 in Appellant's disclosed prior art might replace QPSK spreading circuit 102 in SATO. However, this also would not result in the combination recited in Appellant's claims.

As set forth above, the only explanations of proposed combinations of SATO and Appellant's disclosed prior art in the record are those provided by Appellant. These modifications of SATO with teachings of Appellant's disclosed prior art would simply replace an amplitude adjuster 106 in SATO with amplitude multiplier 406 in Appellant's disclosed prior art, or QPSK spreading circuit 102 of SATO with phase offset calculator 407 in Appellant's disclosed prior art. However, any such replacements/modifications would not result in the combination recited in Appellant's pending claim 25. Further, no alternative arrangement has been proposed by the Examiner, and no alternative arrangement would be obvious to one of ordinary skill in the art such that Appellant's claim 25 would result.

Therefore, no combination of SATO and Appellant's disclosed prior art would result in the combination of Appellant's claim 25. As set forth above, no such combination of SATO and Appellant's disclosed prior art results in Appellant's claimed invention, and the rejection of Appellant's claim 25 on this ground should therefore be reversed.

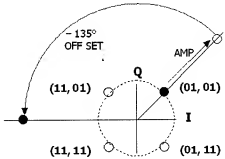
Appellant notes that benefits of the claimed invention were also set forth by Appellant during prosecution, as explanation of what can be accomplished by the claimed invention in terms of reduced signal processing requirements. In this regard, Figure 7 of the present application generally illustrates features of offset processing in 45° units between -135° and 45°.

According to the invention to which Appellant's claim 25 is directed, information (i.e. IQ data) can be represented with two bits prior to amplitude multiplication processing. The two bits are sufficient to identify which of four quadrants QPSK IQ data lies in. Amplitude multiplication can then be performed with respect to the IQ data prior to 45° offset processing. Significant figures are increased. Afterwards, by performing a $\sqrt{2}$ calculation and rounding fractions, the positions of IQ symbol points can be represented with 45° offset applied. Offset processing in 90° units is therefore applied to two-bit information prior to amplitude multiplication.

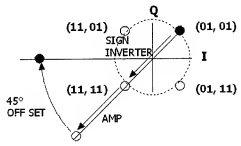
The following illustrations were provided to graphically explain differences in offset processing according to the embodiment of the claimed invention shown in Figure 4A and detailed in Figure 7, in comparison to the prior art shown in Figure 4B (note that the functional differences can be seen by following the directional arrows). As can be seen, simply switching on and off between offset processing in 90° units, by changing the signs of symbol points in Sign Inverter 60, and offset processing in 45° units in 45° Phase Shifters requires only one $\sqrt{2}$ calculation, whereas the Prior Art offset processing requires multiple such $\sqrt{2}$ calculations.

Prior art	(I, Q) →	1. Amplitude Multiplication → 2. -135° Offset
Claimed invention	(I, Q) →	1. 180° Offset (Sign Inverter) → 2. Amplitude Multiplication → 3. +45° Offset (on/off)

PRIOR ART (FIG.4B)



THIS INVENTION (FIG.4A)



Substantively, by inverting the sign, adjusting the amplitude and then providing phase offset, less √2 processing is required than by adjusting the amplitude and then providing a -135° Offset. The reduction in signal processing can be achieved by performing processing in the manner described in Appellant's specification and recited in Appellant's claim 25.

The differences in data to be represented in processing are shown in the following table. The exemplary data for IQ symbol points are explained in tables as follows for the claimed invention in comparison to the prior art shown in Figure 4B:

▼FIG. 4A

INPUT (SCI, SCQ)	OFF SET VALUE	SIGN INVERTER (SRI, SRQ)		AMPLITUDE MULTIPLICATION (AI,	QI)	45°STEP PROCESSING (√2) on/off (RI,	RQ)
(01, 01)	+180	(11, 01)	+180°	SRI * AMP	SRQ * AMP	AI	QI
(01, 01)	-135	(11, 01)		SRI * AMP	SRQ * AMP	AI * cos(45)	QI * cos(45)
(01, 01)	-90	(01, 11)	-90°	SRI * AMP	SRQ * AMP	AI	QI
(01, 01)	-45	(01, 11)		SRI * AMP	SRQ * AMP	AI * cos(45)	QI * cos(45)
(01, 01)	0	(01, 01)	0°	SRI * AMP	SRQ * AMP	AI	QI
(01, 01)	+45	(01, 01)		SRI * AMP	SRQ * AMP	AI * cos(45)	QI * cos(45)
(01, 01)	+90	(11, 11)	+90°	SRI * AMP	SRQ * AMP	AI	QI
(01, 01)	+135	(11, 11)		SRI * AMP	SRQ * AMP	AI * cos(45)	QI * cos(45)

▼FIG. 4B

INPUT (SRI, SRQ)	OFFSET VALUE	AMPLITUDE MULTIPLICATION (AI,	QI)	45°STEP PROCESSING (RI,	RQ)
(01, 01)	+180	SRI * AMP	SRQ * AMP	AI * cos(180)	QI * sin(180)
(01, 01)	-135	SRI * AMP	SRQ * AMP	AI * cos(-135)	QI * sin(-135)
(01, 01)	-90	SRI * AMP	SRQ * AMP	AI * cos(-90)	QI * sin(-90)
(01, 01)	-45	SRI * AMP	SRQ * AMP	AI * cos(-45)	QI * sin(-45)
(01, 01)	0	SRI * AMP	SRQ * AMP	AI	QI
(01, 01)	+45	SRI * AMP	SRQ * AMP	AI * cos(45)	QI * sin(45)
(01, 01)	+90	SRI * AMP	SRQ * AMP	AI * cos(90)	QI * sin(90)
(01, 01)	+135	SRI * AMP	SRQ * AMP	AI * cos(135)	QI * sin(135)

As can be seen, the prior art requires multiple √2 calculations and associated processing where the claimed invention according to Figure 4A and detailed in Figure 7 requires only a single such √2 calculation.

When amplitude multiplication is performed before offset processing in 90° units, as in the Prior Art of Figure 4B, offset processing in 90° units is performed with respect to a greater volume of information than two bits (e.g., 18 bits), and the amount of calculation will necessarily increase. Thus, by performing amplitude multiplication processing after offset processing is performed in 90° units, and before offset processing is performed in 45° units, as in the claimed invention, the processing/calculation amount is reduced in comparison to the prior art shown in Figure 4B. Neither SATO nor Appellant's disclosed prior art is concerned with such signal processing requirements or reductions.

In any event, SATO as modified by Appellant's disclosed prior art does not result in Appellant's claimed invention. Further, modification of SATO that might result in Appellant's

claimed invention is not merely a matter of design choice. Significant calculation and signal processing concerns need to be addressed in ordering sign inverters, phase shifters and amplitude adjusters in the manner of Appellant's claims in comparison with that shown in Appellant's disclosed prior art.

Therefore, according to the presently claimed invention, amplitude multiplication processing is performed after offset processing in 90° units, and before performing 45° offset processing, for the reasons described above, and the manner of this processing is not an obvious variation that one of ordinary skill in the art would have been led to by SATO and/or Appellant's disclosed prior art.

Claim 26

Claim 26 is patentable over SATO in view of Appellant's disclosed prior art for reasons similar to the above-noted reasons set forth as to the allowability of claim 25. The combination of features recited in independent claim 26 are not disclosed, suggested or rendered obvious by the teachings SATO in view of Appellant's disclosed prior art. In this regard, with respect to the summary explanation above of the teachings SATO in view of Appellant's disclosed prior art, SATO in view of Appellant's disclosed prior art does not disclose, suggest or render obvious a signal point mapper for mapping a QPSK modulation signal in a phase space, comprising: a sign inverter that inverts a sign of the QPSK modulation signal to obtain a first phase offset of a multiple of 90°; an amplitude adjuster that adjusts an amplitude of a signal output from the sign inverter; and a phase offsetter that provides a second phase offset smaller than 90° to a signal output from the amplitude adjuster, as recited in claim 26.

That is, similar to claim 25, the rejection of claim 26 is improper in that amplitude adjustment in claim 26 is performed after offset processing in 90° units, and before performing 45° offset processing, for the reasons described above, and the manner of this processing is not an obvious variation that one of ordinary skill in the art would have been led to by SATO and/or Appellant's disclosed prior art.

Claim 27

Claim 27 is also patentable, at least for the reason that this claim depends from an allowable claim 26, respectively, and because this claim recites additional features that further define the invention to which claim 26 is directed. Further, claim 27 is separately patentable over SATO in view of Appellant's disclosed prior art, which fails to disclose, suggest or render obvious Appellant's claimed combinations including, inter alia:

the signal point mapper according to claim 26, the phase offsetter comprising: a fixed phase offsetter that provides a predetermined amount of a fixed phase offset, wherein the phase offsetter controls a total phase offset amount with the phase offset implemented by the sign inverter to become a desired offset amount.

Claim 28

The combination of features recited in independent claim 28 are also not disclosed, suggested or rendered obvious by the teachings SATO in view of Appellant's disclosed prior art. In this regard, with respect to the summary explanation above of the teachings SATO in view of Appellant's disclosed prior art, SATO in view of Appellant's disclosed prior art does not disclose, suggest or render obvious a CDMA transmission apparatus for controlling a phase and

amplitude of a transmission signal by closed-loop control, comprising: a signal point mapper having: a sign inverter that inverts a sign of a QPSK modulation signal to obtain a first phase offset of a multiple of 90°; an amplitude adjuster that adjusts an amplitude of a signal output from the sign inverter; and a phase offsetter that calculates a second phase offset smaller than 90° with a signal output from the amplitude adjuster; and a transmission controller that provides control information to the signal point mapper based on a message included in a reception signal from a receiver that receives communication signals from the CDMA transmission apparatus, as recited in claim 28.

That is, similar to claims 25 and 26, the rejection of claim 28 is improper in that amplitude adjustment in claim 28 is performed after offset processing in 90° units, and before performing 45° offset processing, for the reasons described above, and the manner of this processing is not an obvious variation that one of ordinary skill in the art would have been led to by SATO and/or Appellant's disclosed prior art.

Further, SATO in view of Appellant's disclosed prior art does not disclose, suggest or render obvious the features relating to a message included in a reception signal from a receiver that receives communication signals from a CDMA transmission apparatus, as recited in claim 28. There is no feature of SATO or Appellant's disclosed prior art that discloses controlling the second phase offsetting based on a signal from a remote source. At no time has the Examiner established that any combination of SATO and Appellant's disclosed prior art would result in such features. Accordingly, the rejection of claim 28 is improper and should be withdrawn for these additional reasons.

Claims 29-31

Claim 29-31 are also patentable, at least for the reason that these claims depend from an allowable claim 28, respectively, and because these claims recite additional features that further define the invention to which claim 28 is directed. Further, claims 29-31 are separately patentable over SATO in view of Appellant's disclosed prior art, which fail to disclose, suggest or render obvious Appellant's claimed combinations including, inter alia:

(i) *the CDMA transmission apparatus according to claim 28, the phase offsetter comprising: a fixed phase offsetter that provides a predetermined amount of a fixed phase offset* (claim 29);

(ii) *the CDMA transmission apparatus according to claim 28, wherein the phase and amplitude can be controlled for every transmit channel* (claim 30); and

(iii) *the CDMA transmission apparatus according to claim 29, wherein the phase and amplitude can be controlled for every transmit channel* (claim 31).

Claim 33

The combination of features recited in independent claim 33 are also not disclosed, suggested or rendered obvious by SATO in view of Appellant's disclosed prior art. In this regard, with respect to the summary explanation above of the teachings of SATO in view of Appellant's disclosed prior art, SATO in view of Appellant's disclosed prior art do not disclose, suggest or render obvious a phase offsetter, comprising: a sign inverter that inverts a sign of signed binary data to obtain a first phase offset of a multiple of 90°; and a phase shifter that calculates a phase shift to provide the sign-inverted signed binary data a phase offset smaller

than 90°, and that provides the sign-inverted signed binary data the phase offset smaller than 90° based on a control signal from a remote source, as recited in claim 33.

That is, similar to claim 28, SATO in view of Appellant's disclosed prior art also does not disclose, suggest or render obvious features of controlling the second phase offsetting based on a signal from a remote source. There is no feature of SATO or Appellant's disclosed prior art that discloses controlling second phase offsetting based on a signal from a remote source. At no time has the Examiner established that any combination of SATO and Appellant's disclosed prior art would result in such features. Accordingly, the rejection of claim 33 is improper and should be withdrawn for these additional reasons.

Claims 34-35

Claims 34-35 are also patentable, at least for the reason that these claims depend from an allowable claim 33, respectively, and because these claims recite additional features that further define the invention to which claim 33 is directed. Further, claims 34-35 are separately patentable over SATO in view of Appellant's disclosed prior art, which fail to disclose, suggest or render obvious Appellant's claimed combinations including, inter alia:

(i) *the phase offsetter according to claim 33, further comprising: at least one switch used to provide the sign-inverted signed binary data the phase offset smaller than 90° based on the control signal from the remote source* (claim 34); and

(ii) *the phase offsetter according to claim 33, wherein, when a phase and an amplitude of the signed binary data are adjusted, the sign of the signed binary data is inverted before the amplitude of the sign inverted binary data is adjusted* (claim 35).

(8) CONCLUSION

For at least the reasons set forth above, each and every pending claim of the present application meets the requirements for patentability under 35 U.S.C. §103(a), and the present application and each pending claim thereof is allowable over the prior art of record. Accordingly, the Board of Patent Appeals and Interferences is respectfully requested to reverse the Examiner's decision to reject claims 25-31 and 33-35.

If there are any questions about this application, any representative of the U.S. Patent and Trademark Office is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,
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CLAIMS APPENDIX

25. A phase offset calculator, comprising:

a sign inverter that inverts a sign of signed binary data to obtain a first phase offset of a multiple of 90°;

an amplitude adjuster that adjusts an amplitude of a signal output from the sign inverter; and

a phase offsetter that provides a second phase offset smaller than 90° to a signal output from the amplitude adjuster.

26. A signal point mapper for mapping a QPSK modulation signal in a phase space, comprising:

a sign inverter that inverts a sign of the QPSK modulation signal to obtain a first phase offset of a multiple of 90°;

an amplitude adjuster that adjusts an amplitude of a signal output from the sign inverter; and

a phase offsetter that provides a second phase offset smaller than 90° to a signal output from the amplitude adjuster.

27. The signal point mapper according to claim 26, the phase offsetter comprising:

a fixed phase offsetter that provides a predetermined amount of a fixed phase offset,

wherein the phase offsetter controls a total phase offset amount with the phase offset implemented by the sign inverter to become a desired offset amount.

28. A CDMA transmission apparatus for controlling a phase and amplitude of a transmission signal by closed-loop control, comprising:

a signal point mapper having:

a sign inverter that inverts a sign of a QPSK modulation signal to obtain a first phase offset of a multiple of 90°;

an amplitude adjuster that adjusts an amplitude of a signal output from the sign inverter; and

a phase offsetter that calculates a second phase offset smaller than 90° with a signal output from the amplitude adjuster; and

a transmission controller that provides control information to the signal point mapper based on a message included in a reception signal from a receiver that receives communication signals from the CDMA transmission apparatus.

29. The CDMA transmission apparatus according to claim 28, the phase offsetter comprising:

a fixed phase offsetter that provides a predetermined amount of a fixed phase offset.

30. The CDMA transmission apparatus according to claim 28,

wherein the phase and amplitude can be controlled for every transmit channel.

31. The CDMA transmission apparatus according to claim 29,

wherein the phase and amplitude can be controlled for every transmit channel.

33. A phase offsetter, comprising:

a sign inverter that inverts a sign of signed binary data to obtain a first phase offset of a multiple of 90°; and

a phase shifter that calculates a phase shift to provide the sign-inverted signed binary data a phase offset smaller than 90°, and that provides the sign-inverted signed binary data the phase offset smaller than 90° based on a control signal from a remote source.

34. The phase offsetter according to claim 33, further comprising:

at least one switch used to provide the sign-inverted signed binary data the phase offset smaller than 90° based on the control signal from the remote source.

35. The phase offsetter according to claim 33,

wherein, when a phase and an amplitude of the signed binary data are adjusted, the sign of the signed binary data is inverted before the amplitude of the sign inverted binary data is adjusted.

EVIDENCE APPENDIX

None

RELATED PROCEEDING APPENDIX

None